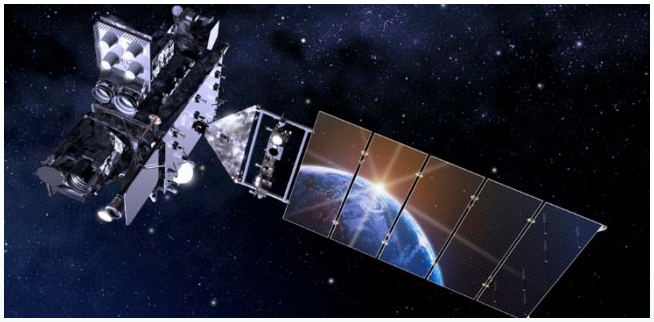


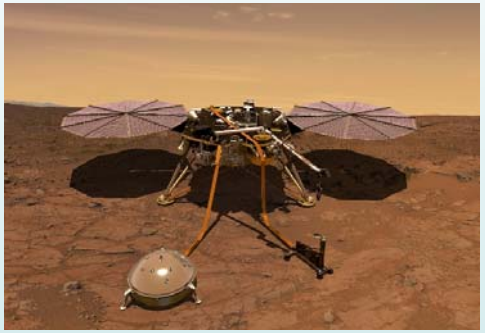
NOAA's GOES-16 weather satellite to showcase its lightning detection capabilities
Artist's rendering of the GOES-16 satellite in orbit.

Image Credit: NOAA

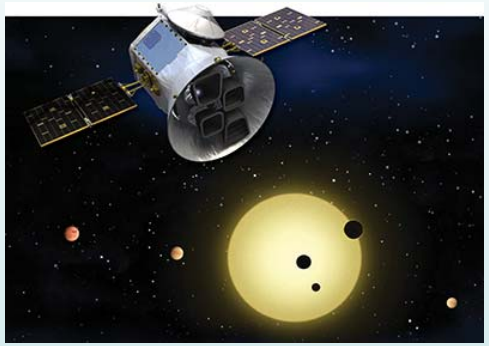
National Aeronautics and Space Administration

NASA

NASA/NEPAG Experience with DLA Audits – Panel Discussion



This artist's concept depicts the stationary NASA Mars lander known by the acronym InSight at work studying the interior of Mars. *Image Credit: NASA/JPL-Caltech*



The Transiting Exoplanet Survey Satellite (TESS) is a planned space telescope for NASA's Explorers program, designed to search for exoplanets. *Image Credit: NASA*

Shri G. Agarwal
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California Institute of Technology
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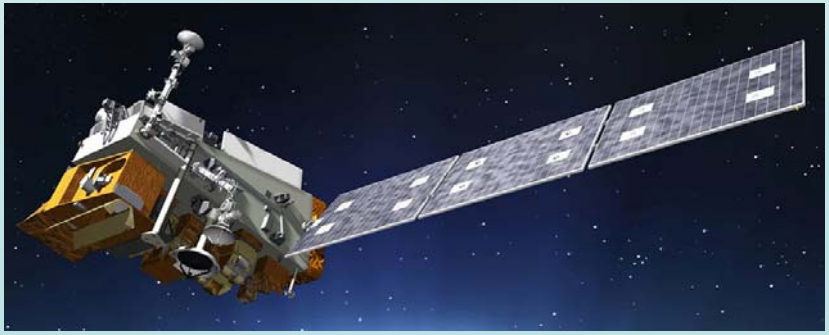
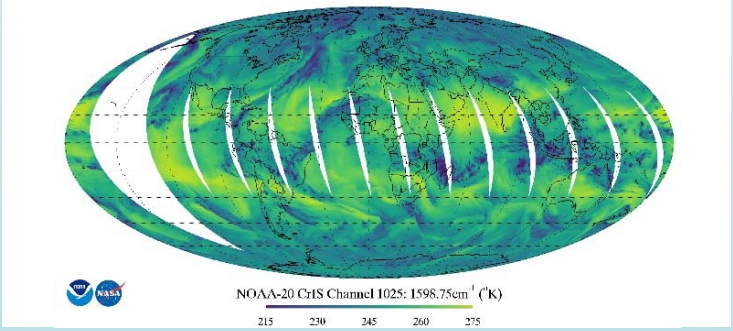
818-354-5598



This illustration depicts the Joint Polar Satellite System-1, or JPSS-1, spacecraft designed to provide forecasters with crucial environmental science data to provide a better understanding of changes in the Earth's weather, oceans and climate. *Image Credit: Ball Aerospace*



First Image on science data from JPSS-1.

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NEPAG and DLA Audits

- The Defense Logistics Agency (DLA) is the designated DoD entity with **authority to approve or disapprove suppliers**. They audit over 150 QML/QPL suppliers (and their supply chains) every year. NASA supports about 25% of the audits conducted by DLA.
- The goal of a DLA audit is to verify overall compliance with the applicable requirements independently and objectively to produce reliable standard products.
- What the Agencies like NASA, Air Force, and NRO bring to the audits is their **technical expertise**. Audit support is **decided on the NEPAG telecons**. A high-level summary of audit results is entered into the NASA **SAS** (Supplier Assessment System) database.
- These audits can be viewed as a multi-pronged effort: we support them as subject matter experts, gain personal knowledge, make contacts**, and also help resolve any current flight project issues with that supplier**.
- Unlike the old days of one stop audits, the audits of today focus on supply chain management and approval of various companies specializing in die design, wafer fabrication, assembly, electrical testing, column attach, etc. ESD/handling takes on an increasingly important role (more stops—more places with risk). RTG4 FPGA example:
  - Die design: Microsemi, San Jose, CA
  - Wafer fabrication: UMC, Singapore, and UMC, Tainan, Taiwan
  - Assembly and Test: Kyocera, San Diego, CA
  - Burn-in: ISE, San Jose, CA
  - Column attachment: Six Sigma, Milpitas, CA
  - Electrical test: Microsemi, San Jose, CA

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A Changing Landscape (Shipping/Handling/ESD Challenge)

A New Trend – Supply Chain Management
Ensuring gap-free alignment for each qualified product
(All entities in the supply chain must be certified/approved)

Manufacturer A	Die design
Manufacturer B	Fabrication
Manufacturer C	Wafer bumping
Manufacturer D	Package design and package manufacturing
Manufacturer E	Assembly
Manufacturer F	Column attach and solderability
Manufacturer G	Screening, electrical and package tests
Manufacturer H	Radiation testing

More Stops — More Places with ESD Risk

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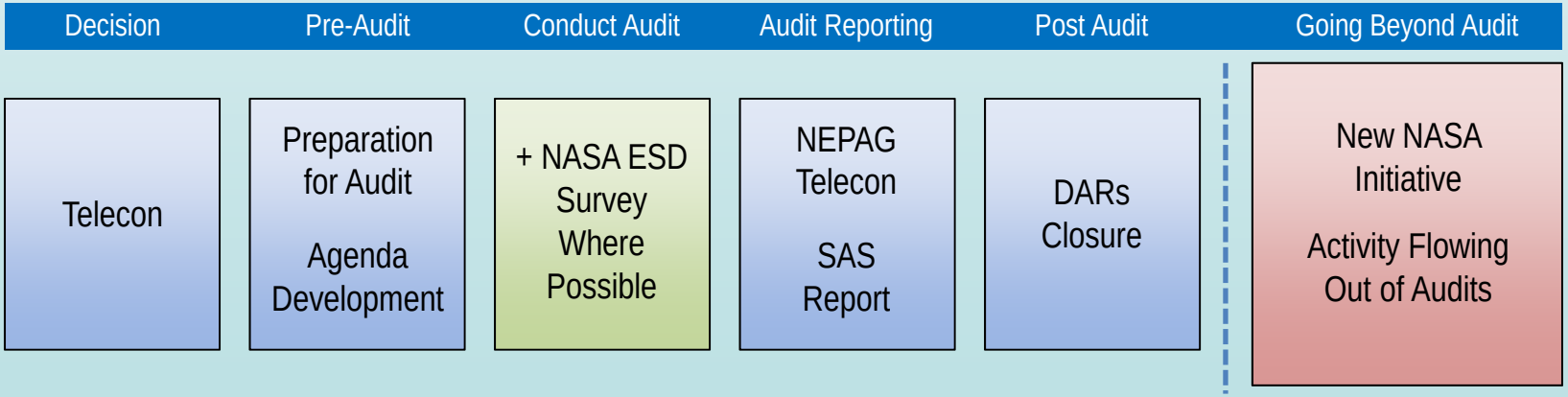
NASA's DLA Audit Support Process

- **Audits**
  - Decided on during NEPAG telecons
  - Audits preparation
  - Arrange for NASA ESD survey (when possible)
  - Report audit results on NEPAG telecon
  - Submit SAS form
  - DARs closeout
  - Going beyond audits
    - ❖ New initiative by NASA
    - ❖ Activity flowing out of audits (see next few slides)

NEPAG Audit Process



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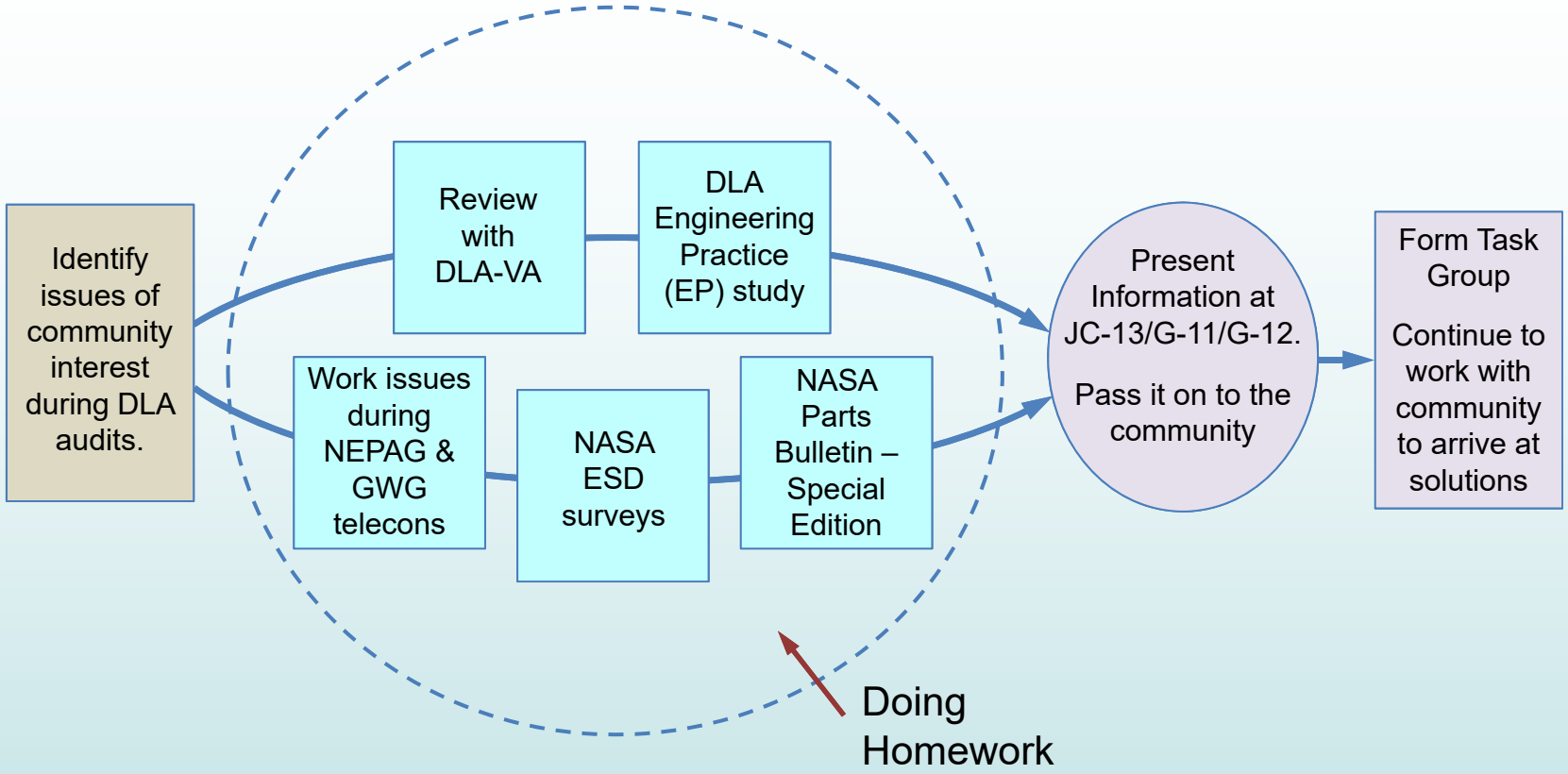
Resolving Major Issues Found During DLA Audits

- **The Paths from Issues to Microcircuit Process Improvements**
- NASA, Aerospace Corporation, and other organizations often participate along with the Defense Logistics Agency (DLA) Land and Maritime personnel in DLA audits. The primary purpose of DLA audits is to get better electronic parts by monitoring compliance with the MIL specifications and by working with the manufacturers to enhance quality of their products.
- In addition, NASA has conducted electrostatic discharge (ESD) surveys of parts manufacturers. Those surveys produced recommendations regarding ESD mitigation and control. These recommendations are not enforced, but the surveyed companies all implemented the suggestions.
- However, as shown on the next slide, there is much more that comes from these audits and surveys. These visits help identify concerns and/or opportunities that are then addressed by other means. This is a path that has worked in resolving major issues found during the audits and surveys that may require community involvement. It may evolve or be adjusted over time.

NEPAG

Taking Audit Findings a Step Further!



- Bring general awareness (Via NASA Bulletins, Surveys)
- Work with DLA to conduct engineering practice (EP) study
- Generate a basic proposal and related information so the potential task group (TG) has a strong starting point.
- This path has **saved time** in resolving major issues found during audits.

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Taking Audit Findings a Step Further!
Issues from Microcircuit / Other Audits and Methods of Resolution

Audits						
Class Y	New Technology Infusion		NASA Parts Bulletin	DLA Engineering Practice (EP) study	CE-12 Task Group (TG)	MIL-PRF-38535 Revision K
Burn-in	Varied interpretations of requirements			DLA Engineering Practice (EP) study	JEDEC Task Group (TG)	JEP163. TG still open
Underfill	Difficulties in meeting requirements		NASA Parts Bulletin – Special Edition on Underfills	DLA Engineering Practice (EP) study	JEDEC Task Group	Resolved
ESD	Old/inconsistent requirements (e.g. 3 zaps vs 1 zap per pin)	NASA ESD Surveys	NASA Parts Bulletin – Special ESD Edition	DLA Engineering Practice (EP) study	DLA presented EP results in January 2017	JC-13 ESD task group formed
Crystal Oscillators	Per manufacturers, practically no sales for QPLS oscillators		NASA Parts Bulletin – in preparation	DLA EP study planned	DLA talk at Space meeting last September	New issue

Process Flow:

*DLA Audits: Major issues uncovered during DLA audits

*NASA Parts Bulletin – Special Edition: Gives subject matter background. Provides results of NASA evaluations, ESD surveys, etc.

*DLA EP Study: A large survey of manufacturers, users, others.

*JEDEC/CE-11/CE-12 Meetings: Where discussions are held.

Conducting NASA ESD Surveys concurrently with DLA Audits Teledyne-e2v Grenoble, FR

- Teledyne-e2v (T-e2v) makes advanced microcircuits, such as microcontrollers and high speed (Gsps) A/D and D/A converters. Their products are used at JPL and other NASA centers.
- DLA invited us to support T-e2v's audit: re-audit for QML Classes Q, V and initial audit for Class Y. We worked with DLA and the company to add NASA ESD survey to the agenda. 514 and 512 joined hands to support this trip.
- This was a useful effort.
- The audit and survey findings were reviewed with the company, none major: some related to their PIDTP, their use of cloth wrist wraps, etc.
- We'll schedule a Learn@Lunch Webinar with the company.

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FY18 YTD Listing of NASA Supported DLA Audits (18), and NASA ESD Surveys (8); Concurrently Done: 2

← Audit →						← NASA ESD Survey →			
DLA Audit Date Week of	NASA Auditors	Center	Audit SAS	Company	Location	NASA ESD Survey Participants	Survey Date	ESD SAS	Notes
				MSK, Anaren	Syracuse, NY	Monroe (LaRC)	Done 10-11-17		Multi-center usage
				Kyocera	San Diego, CA	Nelson, Agarwal, Do	Done 10-23-17	Done	Q, V, Y assembly for major mfrs
				DDC	San Diego, CA	Nelson, Agarwal	Done 10-24-17	Done	Q, V, Moved
Nov 13, '17	Haggquist	GSFC	REC	Amphenol	Sydney, NY				
Nov 13, '17	Damron	MSFC		Scientific Coating	Santa Clara				
Nov 13, '17	Damron	MSFC		UHV Splittering	Santa Clara				
Nov 27, '17	Agarwal	JPL	Yes	Microsemi	San Jose, CA	Nelson	Done 5-15-18	Done	Q, V, RTG4
Nov 27, '17	Majewicz	LaRC	REC	Cobham	Plainview, NY				
Dec 4, '17	Rosal	GSFC		Positronic	Mt Vernon, MO				
Dec 4, '17	Agarwal	JPL	Yes	AIMS	Pune, India				
Dec 4, '17	Agarwal	JPL	Yes	AII	Pune, India				
Dec 11, '17	Agarwal	JPL	Yes	Positronic	Pune, India				
Dec 11, '17	Damron	MSFC		SST Corp	Billerica, MA				
Jan 22, '18	Gutierrez	JPL		Amp Fiber	Allen, TX				
Jan 29, '18	Agarwal	JPL	REC	Cobham	COS, CO	Nelson, Agarwal	Done 2-1-18	Done	Q, V, in Y Qual. (Coord w/DLA audit)
Jan 29, '18	Majewicz	LaRC		Henkel	Rancho Dominguez, CA				
Feb 12, '18	Agarwal	JPL	REC	Micross	Orlando, FL	Nelson	Done 5-1-18	Done	Q, V, FRAM for Cypress
				Micross	Raleigh, NC	Nelson, Do	Done 5-3-18	Done	Wafer Bump., IBM-like Col attach
Mar 5, '18	Majewicz	LaRC		IR	San Jose, CA				
Mar 5, '18	Gutierrez	JPL		Cirexx	San Jose, CA				
Mar 12, '18	Agarwal	JPL	REC	Teledyne-e2V	Grenoble, FR	Do, Agarwal	Done 3-15-18	Done	Q, V, initial Y. (Coord w/DLA audit)
Mar 15, '18	Agarwal, Martinez	JPL		Q-Tech	Culver City, CA	TBD	TBD		
				Isovac	Glendale, CA	JPL/MSFC	TBD		Kr tester had plastic tubes

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Staying Out of Harm's Way
Example: Audit of ITT Cannon in Nogales Mexico

- When DLA conducts audits in designated countries, they get DoD security coverage. However, this security is not guaranteed for other auditors (NASA and Air Force are supposed to make their own arrangements).

- The U. S. State department website shows a high risk level for this region.

- NASA has not been supporting these audits due to security concerns for its auditors.

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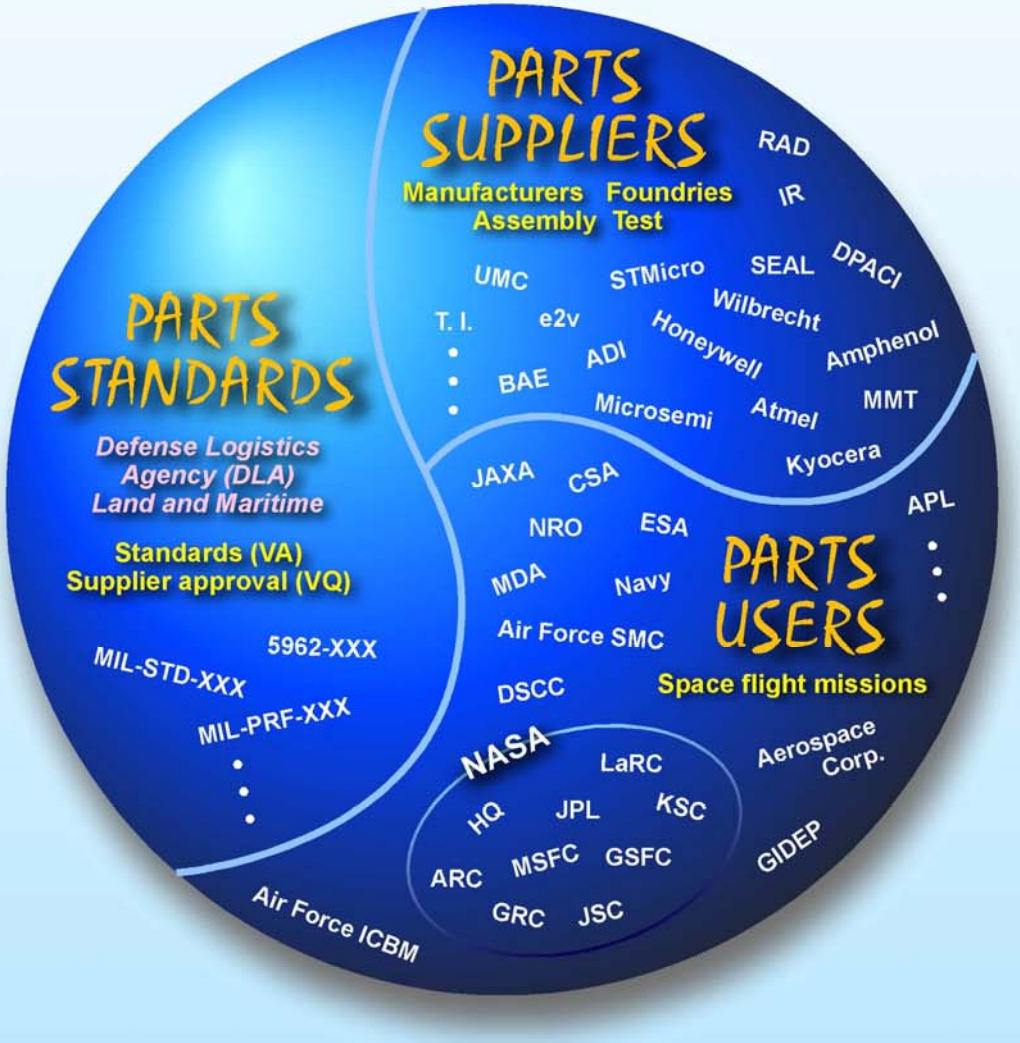
Wafer Fab Audits

- Background:
  - DLA on September 29, 2017 issued a letter: “Evaluation of DLA Land and Maritime – VQ workload.” This DLA letter (copy attached) described the rationale and attempted to justify a 6-month moratorium on audits of semiconductor wafer fabrication facilities. The moratorium began on September 1, 2017. The intent of the moratorium was to re-assign increasingly limited DLA resources while balancing risks over the wide range of devices overseen by DLA-VQ, the auditing branch of DLA.
- NASA Action:
  - The U. S. Agencies including NASA’s NEPAG program, and parts manufacturers expressed grave concerns over this moratorium. DLA said that they were still awaiting a few more inputs. NASA HQ sent a letter to DLA management.
- Status:
  - In their May 2, 2018 letter, DLA lifted the moratorium. DLA-VQ will establish a working group to review the wafer fabrication audit process to ensure proper balance of workload, resources, frequency of follow on audits and supply chain risk.

Wafer Fabrication Requirements

- As part of QML certification, the manufacturer must demonstrate wafer fabrication capability which consists of the fabrication sequence, design rules, electrical characteristics, and process information. All supporting documentation and data shall be made available to the qualifying activity (which is DLA, Aerospace, and NASA/JPL).
- The program to contain test structures needed to characterize a technology's susceptibility to intrinsic reliability failure mechanisms such as electromigration, time dependent dielectric breakdown (TDDB), etc. The wafer fabrication sequence to produce finished wafers shall be established with processing limits for each wafer fabrication step.
- In addition to the requirements called out in MIL-PRF-38535, we have added the following specific checks:
- For high speed devices, we have added hot spots evaluation.
- Extrapolation of commercial data to the military temperature range
- Counterfeit mitigation for masks produced by third party vendors
- ESD Requirements
  - Differing interpretations: Auditors think the requirements of MIL-STD-38535 apply to foundries, the fabs have disagreed. (This is being fixed in Rev. L of 38535)
  - Audits of incoming and outgoing areas have caused ESD concerns
  - A lack of stringent ESD program can cause latent damage
- We were strongly opposed to the moratorium because it increased the risk of reliability problems and eliminated critical knowledge interchange in the supply chain. The die is the functional component of the semiconductor device and errors made in die fabrication cannot be removed by later processes in the manufacturing flow.

Space Parts World
Develop/Maintain Standards for Space Electronic Parts



The parts users and standards organizations work with suppliers to ensure availability of standard parts for NASA, DoD and others. **For Space microcircuits, DLA, NASA/JPL (S. Agarwal) and the U.S. Air Force / Aerospace Corp. (L. Harzstark) form the Qualifying Activity (QA).**

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Partnering

JEDEC JC-13 (Manufacturers)

JC-13	Solid State Devices for Government Products
JC-13.1	Discrete Semiconductors for Government Products
JC-13.2	Microelectronics for Government Products
JC-13.4	Radiation Hardness
JC-13.5	Hybrids and Multi-chip Modules for Government Products
JC-13.7	New Electronic Device Insertion for Government Products

Joint meetings held
3 times a year

SAE CE-11/CE-12 (Industry/Space Users, Primes, Subs)

SAE CE-11	Users of Passive Components
SAE CE-12	Users of Solid State Devices
	CE-12 Management:
	Chair – A. Touw
	Vice Chair – (JPL) S. Agarwal
SAE CE-11 & CE-12	Space Subcommittee Chair – (JPL) S. Agarwal

NASA Centers:

ARC
GRC
GSFC
JPL
JSC
KSC
LaRC
MSFC

Weekly Telecons
(Domestic)

Monthly Telecons
(International)

Partners from Outside NASA:

Domestic
- JHU/APL, Others
- The Aerospace Corp,
- U.S. Air Force, U.S. Navy,
- U.S. Army, DLA,

International
- ESA, JAXA, CSA

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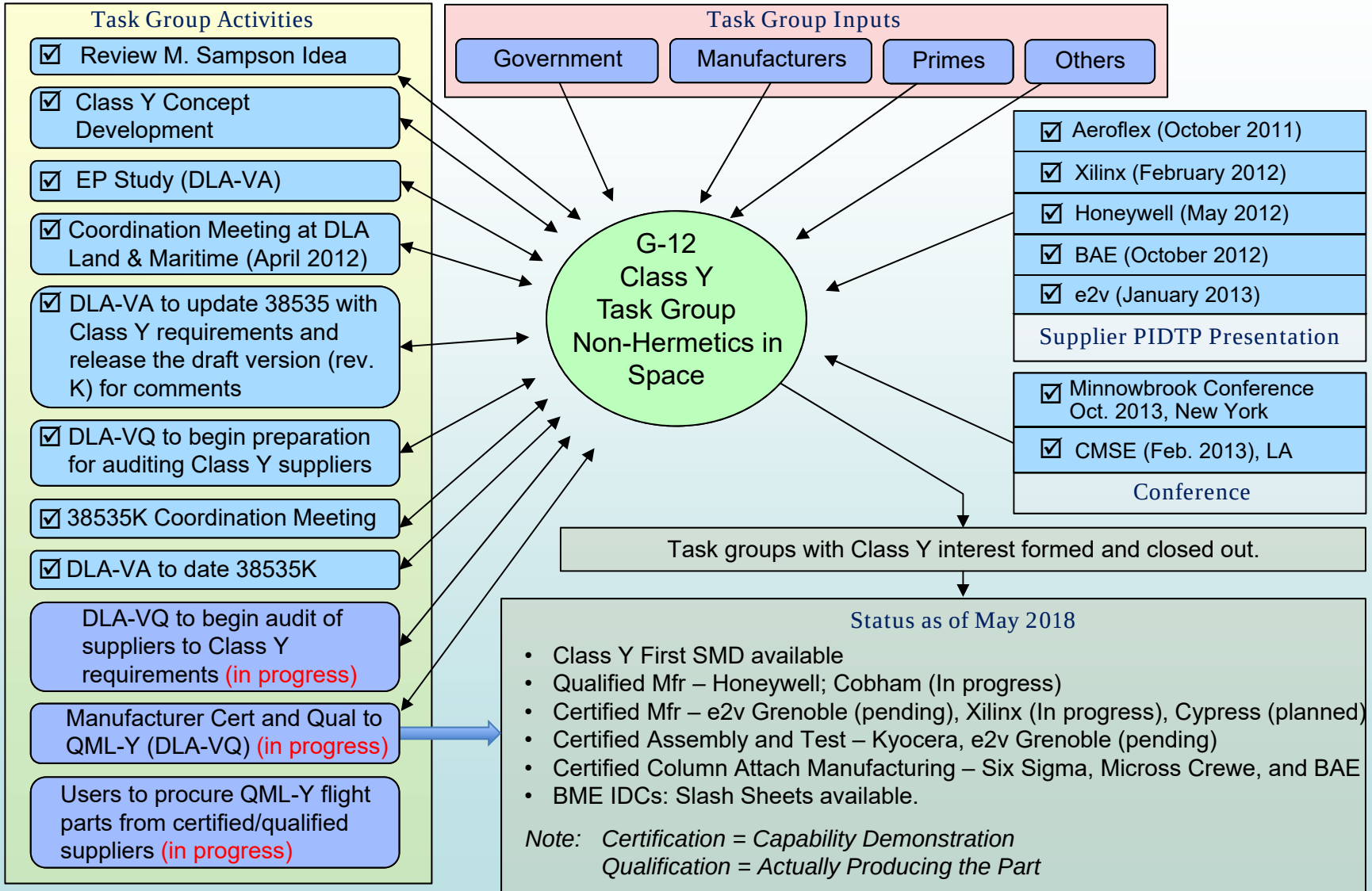
Infusion of the New Class (Y) Technology into the QML System for Space (Status May2018) – shows audits activity



BGA / CGA = Ball-Grid Array / Column-Grid Array
BME = Base Metal Electrode
IDC = Inter Digitated Capacitor

PIDTP = Package Integrity Demonstration Test Plan
SMD = Standard Microcircuit Drawing

First Released SMD for Class Y Part

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Preliminary
Last updated
5/9/17

Class Y SMD

(Class Y Ceramic non hermetic flip chip LGA devices)

REV																		
SHEET																		
REV																		
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33

REV STATUS	REV													
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY Muhammad A. Akbar	
	APPROVED BY	MICROCIRCUIT, CERAMIC NON HERMETIC FLIP CHIP, DIGITAL, CMOS SOI, GATE ARRAY HX5000, RADIATION HARDENED, MONOLITHIC SILICON
	DRAWING APPROVAL DATE	
AMSC N/A	REVISION LEVEL	SIZE A / CAGE CODE 67268 / 5962-17B01
		SHEET 1 OF XX

DSCC FORM 2233
APR 97

5962-EXXX

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: XX-XX-XX

Approved sources of supply for SMD 5962-17B01 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Standard microcircuit drawing PIN 1/ 2/	Vendor CAGE number	Vendor similar PIN
5962H17B0106YXC	34168	HX518X
5962H17B0106YYC	34168	HX518Y

1/ Microcircuits devices supplied to this drawing are land grid array (LGA) packages with lead finish mark letter C (gold). However,for future AID drawing column grid array (CGA) or ball grid array (BGA) packages terminal lead finish mark shall be provided with "F".

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell Aerospace - Plymouth 12001 Highway 55 Plymouth, MN 55441-4744

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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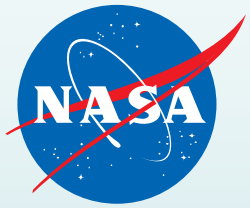
http://nepp.nasa.gov



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